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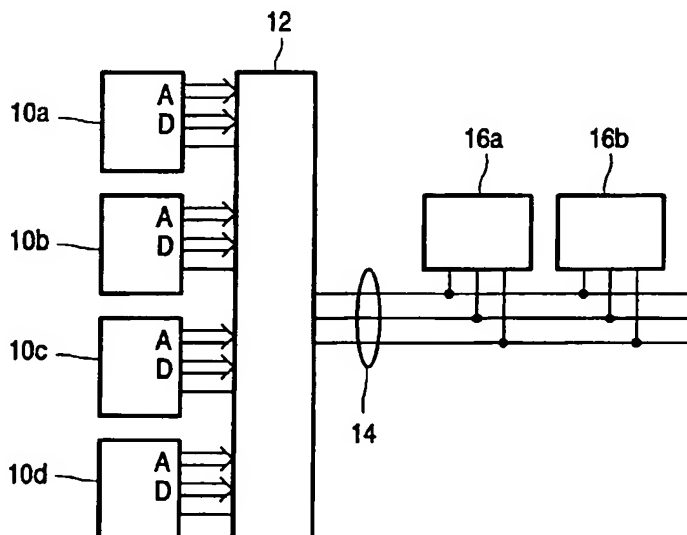
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(54) Title: **ELECTRONIC DATA PROCESSING CIRCUIT THAT TRANSMITS PACKED WORDS VIA A BUS**



(57) Abstract: An electronic data processing circuit contains a plurality of data handling units (10a-d, 16a-b) with data outputs, at least part of the data handling units having address outputs. The data handling units supply words of preferably selectable size to a bus. A bus controller (20) is arranged to control access to the bus in successive access cycles. The bus controller (20) causes data bits from a plurality of data words from respective ones of the data handling units (10a-d, 16a-b), to be placed in combination on the data lines in a same bus cycle. The bus controller causes write addresses that the respective ones of the data handling units (10a-d, 16a-b) supply for respective ones of the plurality of data words to be placed on the address lines in a plurality of respective bus cycles. Preferably, the temporal or spatial arrangement of the data words on the bus lines is adapted so as to minimize the number of logic level changes on the bus.



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